Design for manufacturability and reliability of metal bonding for wafer-level MEMS packaging

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Abstract:

The basis for “More-than-Moore” approach in electronics 3D integration is provided by the development of bonding processes for different types of wafers and utilization of through-silicon vias (TSVs). Within the ENIAC Joint Undertaking Lab4MEMS-II project, the Finnish cluster (Aalto University, Okmetic Oyj, Murata Electronics and VTT Techinical Research Centre of Finland) is working on the design and manufacturing for reliable wafer level hermetic interconnection for MEMS/MOEMS devices. Process integration and reliability assessment for “vias before bonding” capping process has been carried out. Contact metallization structures, Poly-Si TSV manufacturing process flow, SLID bonding as well as cap wafer backside processes has been optimized. Different AuSn, CuSn and AlGe based metal bonding metallurgies and their compatibility to Cu, Ni and Pt contact metallizations were studied from manufacturability and reliability viewpoints with dummy wafers. Microstructural and mechanical characterization was carried out on as bonded as well as aged interconnections. Significant differences in mechanical strength and fracture mechanisms were detected between the different combinations of SLID bond materials and thin film structures (i.e. adhesion layers and diffusion barriers). In addition, the observed formation and evolution of interconnection microstructures was rationalized and the effect of the dissolution of contact metallizations to bonding materials on the re-melting temperature of the SLID bond was evaluated.

Presenter:

Dr. Vesa Vuorinen received his M.Sc. degree 1995 in Materials Science and Engineering and D.Sc. degree in 2006 in the Department of Electronics from the former Helsinki University of Technology. Currently he is working as senior university lecturer and project manager in the research group of Electronics Integration and Reliability. His research has been focused on the interfacial reactions encountered in lead-free electronics and reliability of high-density electronics assemblies with emphasis on soldering metallurgy. He has also been responsible for teaching physics of failure and reliability assessment in electronics and direct research cooperation with the industrial partners for the last twenty years. He has been involved in the creation of international electronics assembly technology standards (IEC) and contributed to two text books dealing with interfacial compatibility issues and thermodynamics of solid state diffusion as well as published over 40 scientific papers, 20 conference presentations and several book chapters.